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Schematic Package Supplement

TM

LIBERATOR

Operation, Maintenance, and Service Manual

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SP-200  Sheet 1A
1st Printing
**MEMORY MAP**

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**Schematic Reference Designators and Symbols**

Logic symbols depict the logic function performed by that particular device and may differ from the manufacturer's data.

**REFERENCE DESIGNATORS:**

- C: Capacitor
- CR: Diode, signal or rectifier
- F: Fuse
- J: Connector
- L: Inductor, fixed or variable
- LS: Speaker
- P: Connector
- Q: Transistor or silicon-controlled rectifier
- R: Resistor, fixed or variable
- S: Switch
- T: Transformer
- TP: Twisted wire pair
- VR: Voltage regulator
- Y: Crystal

**WIRE COLORS:**

- R: Red
- GN: Green
- Y: Yellow
- W: White
- BU: Blue
- BN: Brown
- BK: Black
- OR: Orange
- V: Violet
- QY: Gray

Electrical components shown on the schematic diagrams are in the following units unless otherwise noted:

- Capacitors = microfarads (µF)
- Resistors = ohms (Ω)
- Inductors = microhenrys (µH)

**SYMBOLS:**

- Ground
- PCB edge connector pad
- Test Point
- PCB test connector pad

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To avoid faulty readings while testing signatures, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the entire test.

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Liberator™ PCB Schematic Diagram

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SP-309 Sheet 58
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Description of Liberator PCB Signal Names

A0-A15
Address bits on Microprocessor Address Bus lines A0-A15 are software-generated by Microprocessor C2. When BITMD is low, A0-A15 are applied through buffers B1 and E1 to produce the bits on A00-A15.

A80-A93, A91
Address bits on Buffered Microprocessor Address Bus lines A80-A93 are software-generated either by Microprocessor C2 or by BITMD and F1. When BITMD is low, the bits on A80-A93 are generated via buffers B1 and E1. When BITMD is high, BITMD and F1, low, the bits on A80-A93 are the sum of lines A80-A93 and P90-P91.

BITMD
The Bit Mode Enable signal is software-generated at pin 8 of BITMD Map Address Decoder D4 during address 0002. BITMD is the output control signal for BIT Map Decoders H1 and F1. When BITMD goes low, the data bits latched by H1 and F1 from D80-D87 on the last positive-going transitions of XCKD and XCKD are, on lines A80-A93 and P90-P91.

BITMD
If the Bit Mode Disable signal is software-generated at pin 8 of the invert F4 pin on the BIT Map Address Decoders circuit during address 0002. BITMD is the diode signal for buffers B1 and E1 of the Microprocessor Circuit. When BITMD goes high, the buffers are tri-stated and the bit map addresses are put on the address bus.

BLU
The Blue signal is a game PCB output signal. BLU is generated at the emitter of Q4 in the Color Control circuit. BLU is latched and stored by Q5 and buffered by Q8 and Q7 to produce BLU.

BMASEL
The Bit Map Address Select signal is hardware-generated at pin 5 of latch F8 in the Refresh circuit. In the Bit Map Address Multiplexers circuit, BMASEL is the A-select signal for BIT Map Address Multiplexers H9, H15, and L11.

B02
The active high level Phase 2 Clock signal is hardware-generated from the internal clock circuit of Microprocessor C2 and buffered by E3. B02 is gated with TR/WB and IF to produce WHITE. WHITE is also used as the clock for custom audio chips B2C and C3D in the Audio Output circuit.

B/W
The Black and White Video signal is a game PCB output signal that is generated at the emitter of Q11 in the Color Out circuit from COMPS, BLU, GRR, and RED. This signal can be used by a black and white video display when a color display is not available.

C3B
The active low level Column Address Select signal is hardware-generated at pin 9 of latch C9 in the Refresh circuit. C3B is used to refresh the column address of the dynamic BIT Map Memories.

C0G-C3C
The bits on Planet Color Code lines C0G-C3C are software-generated by Planet Picture ROMS P8 and M9B.

CURLDCE
The Clear/Load/Write Enable signal is hardware-generated at pin 9 of latch C8 in the Multiplex Clock circuit. CURLDCE is a control signal for the Multiplex Clock circuit.

CONTR
The Coin Counter Left signal is a game PCB output signal generated at the collector of Q3 in the Coin Door and Utility Panel Output circuit. CONTR is applied to the game utility panel to activate the Right Coin Counter.

COLORAM
The active low level Color RAM Enable signal is software-generated at pin 2 of Address Decoder D2 during addresses D99 through D2F and is used in the Color Memory Circuit. When COLORAM is high, the Color Memory addresses bits are from A80-A83. When COLORAM is high and the A select signal is low, the Color Memory address bits are from BITD-BITMD. When COLORAM and the M9B select signal are high, the M9B Memory Address bits are from D80-D87. When both COLORAM and M9B go low, the Color Memories are enabled to write data.

COMPSTY
The active low level Composite Synchronization signal is hardware-generated at pin 3 of gate M3 in the Vertical/ Sync Chain by exclusive-ORing HSYNC and VSYNC. COMPSTY is applied directly to the video display circuitry for further processing.

CTRLD
The active low level Control Load signal is generated at pin 9 of latch T11 in the Coin Counter and LED Output circuit. When CTRLD goes low, counters S11 and N11 are loaded from the Coin Door and Control Panel Input switches.

DC0-DC7
Microprocessor Data Bus lines DC0-DC7 form a bidirectional data bus between the Microprocessor, the Program Memory, and the Audio Output circuits.

DB0-DB7
Buffered Microprocessor Data Bus lines DB0-DB7 form a buffered, bidirectional data bus between microprocessor data bus and microprocessor data bus buffer E2 and BIT Map Decoders H1 and F1. BIT Map Multiplexers H11 and P11, BIT Map Data Buffers H5, S9, and N9, and BIT Map Memories H10, H9, N9, and L10. Longitudinal Scaling latch R8, Color Memories F11, C11, E11, and B11, EROM latches R9 and K2, EROM buffer H2, Coin Door and LED Output decoder T11, and Coin Door and Control Panel input multiplexers R11 and M11.

DIN
The active high level Display Interface signal is generated at pin 8 of gate L4 in the Planet Ram Address Generator Circuit. When high, DIN7 clears counter M7 and (via gate F5) clears latch E8. In the Line Buffer Address Controller circuit, DIN7 clears flip-flop K4 and counter H7.

DISIAT
Disable Data is a active low level signal generated by test equipment connected to the DISIAT test point.

DRAMO-DRAM11
The bits on Bit Map Data Bus lines DRAMO-DRAM11 are software-generated by the Bit Map Memory C2. When BITMD, TR/WB, and R/WB are all low, the bits on DRAMO-DRAM7 are passed through Bit Map Data Buffer T9 to the microprocessor data bus. Otherwise, when BITMD and TR/WB and R/WB are all low, the bits on DRAMO-DRAM7 are multiplexed by S9 and N9 of the Bit Map Data Buffer circuit and passed to lines D80-D87 of the microprocessor data bus.

DRM0
The Bit Map Shift Registers, if LDRST is high, the bits on DRAMO-DRAM11 are used by shift register R9 to produce BITD; the bits on DRAMO-DRAM11 are used by shift register R9 to produce BITD; and the bits on DRAMO-DRAM11 are used by shift register R9 to produce BITD. The bits on DRAMO-DRAM11 are used by shift register R9 to produce BITD.

EARCON
The Electrically Alterable Read-Only Memory Control signal is software-generated at pin 4 of Address Decoder D2 at address 69C0. EARCON is the clock signal for latch R2 in the EARCON circuit. When low, EARCON allows R2 to see data bits on lines D50-DB3 to the control lines of EAROM M2.

EARO
The Electrically Alterable Read-Only Memory Read Enable is software-generated at pin 12 of Address Decoder D4 at address 4000. EARO is the select signal for buffer H2 of the EARCON circuit. When low, EARO allows the eight data bits from EAROM M2 to be passed through buffer H2 to the microprocessor data bus.

EARWR
The Electrically Alterable Read-Only Memory Write Enable is software-generated at pin 9 of Address Decoder D2 at addresses 69D9 through 69E3. EARWR is the clock signal for latches P9 and K2 in the EARCON circuit. When low, EARWR allows address bits on lines A80-A85 and data lines on lines D50-DB7 to pass to the address and data input pins of EAROM M2.

FG
The active high level First Segment signal is the carry output of adder R7 in the Longitudinal Scaling Circuit. When FG is high and LDRST is high, the CO of the adder P7 is set. FG is gated with PLS and HDR by gates R4, R8, and P3 in the Planet Ram Address Generator circuit to produce the clock signal for latch N7.

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Description of Liberator PCB Signal Names (continued)

GRN
The green signal is a game PCB output signal developed from the bits on Q8-G2. GRN is generated at the emitter of Q8 in the Color Output circuit. The bits on Q8-G2 are summed at the base of Q9 and buffered by Q8 and Q9 to produce GRN.

HBLANK
The active high-level Horizontal Blanking signal is hardware-generated at pin 11 of counter F9 in the Horizontal Sync Chain. HBLANK is applied through inverter L3 to produce HBLANK. If HBLANK is high when latch T4 is clocked, HBLANK is set high and HBLANK is set low. When HBLANK goes low, HSYNC from latch T4 is preset to the high state.

HBLANK
The active low-level Horizontal Blanking signal is hardware-generated at pin 6 of inverter L3 in the Horizontal Sync Chain by inverting HBLANK. When low, HBLANK prevents HBLANK from coming to pin 6 of latch T4 to the low state and holds latch T4 in the high state. In the Line Buffer Control circuit, when HBLANK goes low, it prevents output from latch T3 from the high state andэрнор to the low state.

HBLANK
The active high-level Delayed Horizontal Blanking signal is hardware-generated at pin 9 of latch T4 in the Horizontal Sync Chain. HBLANK is generated when HBLANK has been delayed by the gated result of bit 1 of ROM. HBLANK is the clock signal for latch M4 in the Vertical Sync Chain.

HBLANK
The active low-level Delayed Horizontal Blanking signal is hardware-generated at pin 8 of latch T4 in the Horizontal Sync Chain. HBLANK is generated when HBLANK has been delayed by the gated result of bit 1 of ROM. HBLANK is the clock signal for latch M4 in the Vertical Sync Chain.

HORL
The Complementary Horizontal Planeti Enable signal is hardware-generated at pin 5 of latch S3 in the Planeti Control circuit. When Horizontal Planeti Enable, HORL is preset to the high state. When latch S3 receives the next positive-going transition of clock 64Hz, HORL is set low. In the Planeti ROM Address Generator circuit, when HORL goes high, it is gated with HBLANK by gate P4 to produce the load signal for counter M7. In the Valid Segment Detector circuit, HORL is the clear signal for latch N3.

HORS
The active high-level Delayed Horizontal Planeti Enable signal is hardware-generated at pin 7 of latch S4 in the Planeti Control circuit. HORL is the high which has been delayed by one cycle of LDRST, HORL, 2Hz, 1Hz, and all remaining output signals from latch S4 are gated by M3, M5, and M4 to produce PLANET, PLANETLD, and PLANETL from latches D9 and H5 in the Planeti ROM Address Generator circuit. When HORL goes high, it is gated with HORL by gate P4 to produce the load signal for counter M7 in the Line Buffer Address Controller circuit. HORL and 4Hz are used to latch S3 and gate J3 to produce INTRST.

HORS
The Complementary Delayed Horizontal Planeti Enable signal is hardware-generated at pin 6 of latch S4 in the Planeti Control circuit. HORL is the complement of HORL, HORL, 2Hz, 1Hz, and all remaining output signals from latch S4 in the Planeti Control circuit are used to generate PLANET, PLANETLD, and PLANETL. When high, HORL is gated with HORL by gate P4 to produce the load signal for latch M7 in the Line Buffer Address Controller circuit. When latch S3 and S4 are driven high, HORS is enabled with HBLANK by gate P3 to the latch S3 in the Valid Segment Detector circuit to produce the clock signal for latch N3.

HSYNC
The Horizontal Synchronization signal is hardware-generated at pin 6 of latch T4 in the Horizontal Sync Chain. HSYNC is generated from 32Hz when latch T4 is clocked by 64Hz. HSYNC is the clock signal for latches H8 and all in the Vertical Sync Chain. HSYNC is also applied directly to the video display circuitry for further processing.

HSYNC
The Complementary Horizontal Synchronization signal is hardware-generated at pin 5 of latch T4 in the Horizontal Sync Chain. HSYNC is generated from 32Hz when latch T4 is clocked by 64Hz. HSYNC is the clock signal for latches H8 and all in the Vertical Sync Chain to produce COMPSYNC.

HSYS
The active low-level Input Switch 0 Enable signal is software-generated at pin 1 of Address Decoder E4 at addresses 5000 through 500F. HSYS is the output control enable signal for multiplexers R11 and M11 in the Coin Door and Control Panel Input circuit. When HSYS is low, HSYNC enables counter S11.

INTACK
The active low-level Interrupt Acknowledge signal is software-generated at pin 3 of Address Decoder S2 at addresses 5600. The signal is acknowledged by hardware from the Interrupt Controller 2 that an interrupt request has been received. INTACK presets latch K3.

I0S
The active low-level Input/Output Sound signal is software-generated at pin 9 of Address Decoder E4 during addresses 7000 through 7700 in the Microprocessor circuit. IOS is gated with the ROM signal by gates H4 and 24Hz to enable bidirectional data bus buffers to pass data. When IOS or ROM is high, data buffer is turned off, which allows custom audio chips 8763 and 8765 to pass data to the microprocessor data bus.

IROCK
The active high-level Interrupt Request Clock signal is hardware-generated at pin 15 of latch M4 in the Vertical Sync Chain. IROCK is the interrupt clock signal for Microprocessor C2.

LATCHEN
The active high-level Latch Enable is generated at pin 1 of gate B6 in the Display Counter and Comparator circuit. LATCHEN is the clock signal for latch A6 in the Display Counter and Comparator circuit and for latch P5 in the Line Buffer circuit.

LBAINC
The active high-level Line Buffer Address Increment signal is generated at pin 16 of J4 flip-flop K4 in the Display Counter and Comparator circuit. In the Line Buffer Address Controller circuit, when LBAINC is high and if either VGA3 or LDRST is high, J4 flip-flop K4 is clocked and counter H7 is enabled to count.

LDRST
The active low-level Load Resteer Enable signal is hardware-generated at pin 8 of Load Resteer Counter Latch K3. When high, LDRST is the shift/load signal for Bit Map Shift Registers R6, P5, and P6 to produce latch R7 in the Planeti Control circuit and the clock signal for latch S3 in the Line Buffer Address Controller circuit.

LSG0-LSG7
The Longitude Scaling bits on lines LSG0-LSG7 are software-generated by Longitude Scaler T7 and S1. These bits are developed from the output signals of the planeti Picture ROMS and the latched data bits from R6. The bits on LSG0-LSG7, together with those from Latitude Scalers P6 and N8, are used by the Multiplanar circuit to produce the bits on lines X0 to X7.

L0X-L0Y, L0X-L0Y
The bits on Display Segment Length lines L0X-L0Y are software-generated from Line Buffer RAMs B7, C7, D7, and E7 in the Valid Segment Detector. L0X-L0Y are used to produce VDPS. In addition, the bits on L0X and L0Y are applied to latch P5 to produce the delayed bits of L0X and L0Y. In the Display Counter and Comparator circuit, the bits on L0X-L0Y, L0X-L0Y, and L0X-L0Y are applied to comparators C6 and C8.

M00-M07
The data bits on Multiplexed Data bus lines M00-M07 are generated by Bit Map Multiplier's H11 and P1 from the data bits on D80-D8F. When BTM goes high, H11 and P1 multiplex the data bits from D80-D8F to produce those on M00-M07. Bit Map Memories E0, T0, P10, L0, F10, S10, and M10 and J0 use the data lines on M00-M07 to generate DRAM-DRAM.

MTR
The Multiplexer signal is generated at pin 7 of shift register S8 in the Multiplexer circuit. MTR is the shift/load enable for shift registers K8 and J6.

MULCLK
The active high-level Multiplanar Clock signal is hardware-generated at pin 8 of gate J4 in the Multiplexer circuit. MULCLK is the clock signal for shift register S8, latch H5, and decoders K5 and J6 in the Multiplexer circuit.

OUT5
The active low-level Output Port 5 signal is software-generated at pin 7 of Address Decoder S2 at address 6000. OUT5 is the enable signal for decoder T11 in the Coin Counter and LED Output circuit.

PIN72
The active low-level Process Initialize signal is generated at pin 6 of gate J3 in the Line Buffer Address Controller circuit. When HBLANK goes low, PIN72 is set low. PIN72 loads counter H7 and preset flip-flop K4 in the Line Buffer Address Controller circuit in the Multiplexer circuit. PIN72 clears latch 6 and D10 in the Valid Segment Detector. PIN72 clears latch N3.

PIN9
The active high-level Pin Bit 0 is software-generated at pin 6 of Bit Map Decoder F1 from the bit on D80 in the Write Protection circuit. PIN9 and PIN10 are multiplexed by C5 to produce WPR in the Bit Map Data Buffers circuit. PIN9 is the A select signal for multiplexers S9 and N9.

PIN1
The active high-level Pin Bit 1 is software-generated at pin 6 of Bit Map Decoder F1 from the bit on D81 in the Write Protection circuit. PIN1 and PIN10 are multiplexed by C5 to produce WPD in the Bit Map Data Buffers circuit. PIN1 is the B select signal for multiplexers S9 and N9.

PLA1
The active low-level Planeti signal is generated at pin 12 of latch T11 in the Coin Counter and LED Output circuit from the data bit on D84. PLA1 is the chip select signal for Planeti Picture ROMS M16/B and T8.
Description of Liberator PCB Signal Names (continued)

PLA2
The Planet 2 Select signal is generated at pin 2 of inverter L5 in the Coin Counter and LED Output circuit by inverting PLA1. PLA2 is the chip select signal for Planet Picture ROMs P6 and R5/16.

PLANET
The Planet Enable signal is generated at pin 6 of flip-flop D9 in the Planet Control circuit. PLANET changes state at a 5-MHz rate, either of the signals at pins 2 or 3 of D6 is high. When high, PLANET is used by latch H5 to produce PLANETL and PLANETLD. When low, PLANET clears flip-flop K4 in the Display Counter and Comparator circuit.

The active-high delayed Planet Enable signal is generated at pin 9 of latch H5 in the Planet Control circuit. When PLANETLD is high and counter D6 of the Display Counter and Comparator circuit has reached its maximum count, gate P4 produces the enable signal for Counter 9. At this time, counter B6 was previously loaded by HIPLAN giving low, counter B6 counting begins to count.

The active-high delayed Planet Enable signal is generated at pin 8 of latch H5 in the Planet Control circuit. When PLANETLD is high and counter D6 of the Display Counter and Comparator circuit has reached its minimum count, gate P4 produces the enable signal for Counter 9. At this time, counter B6 was previously loaded by HIPLAN giving low, counter B6 counting begins to count.

PLAVD/PLAVD3
The Planet Video signals are software-generated by Line Buffers J7 and K7, latched by P6, and applied through multiplexers S5 and T5 to produce the Color Memory address bits.

PLS
The active high-level Planet Segment signal is hardware-generated at pin 8 of latch C8 in the Multiplexer Clock circuit. In the Planet ROM Address Generator circuit, PLS is gated with FSG and H0R by pin R4, R3, and P3 to produce the clock signal for latch N7. In the Multiplexer circuit, PLS is the clock signal for latches F6 and D10.

RAM
The active low-level Random Access Memory enable is software-generated at pin 4 of Address Decoder T2. RAM is gated with A2-A15 by gates D1 and C1 of the Bit Map Address Decoders to produce the enable signal for E4 in the Write Protection circuit. RAM is gated with WRITE to produce the clear signal for latch D5. In the RAM Data Buffer circuit, RAM is gated with BTMD and R/WBY by gate F3 to produce the enable signal for buffer T9.

RAS
The active low-level Row Address Select signal is hardware-generated at pin 8 of latch C8 in the Refresh circuit. RAS is used to refresh the row address of the dynamic Bit Map Memories.

RED
The Red signal is a game PCB output signal developed from the bits on R0-R6. RED is generated at the emitter of Q6 in the Color Output circuit. The bit 2 latch is driven at the base of Q7 and buffered by Q6 to produce RED.

RESET
Reset is an active low-level signal generated at pin 12 of counter J11 from either the Watchdog circuit or the Power-On Reset circuit. The Power-On Reset circuit sets RESET to an active low level either when the RESET test point is shorted to ground or during the time that the power-supply voltages are reaching their stabilized, regulated levels. This ensures that the Microprocessor Address Bus (A0-A15) is stabilized before Microprocessor C2 begins operation.

The Watchdog circuit sets RESET to an active low level if the microprocessor fails to output address before counter J11 has reached its maximum count.

RESET is the clear signal for latches F2 in the EAPROM and T11 in the Coin Counter and LED Output circuit.

ROM
The active-high Read-Only Memory Enable signal is software-generated at pin 8 of gate H4 in the Address Decoders circuit during addresses B000 through BFFF. In the Micropocessor circuit, ROM is gated with VGS by gates G4 and H3 to enable bidirectional data bus buffer E2 to pass data.

In addition, ROM is ANDed with CRRT by gate H4 in the Program Memory circuit to enable buffer F2 to pass data.

ROM0
The active-low Read-Only Memory Chip Select 0 signal is software-generated at pin 12 of Address Decoder T3 during addresses 0000 through 0FFF. ROM0 is the chip-select signal for Program Memory R5/1. When low, ROM0 allows R1/1 to be addressed and to pass data to buffer F2.

ROM1
The active-low Read-Only Memory Chip Select 1 signal is software-generated at pin 11 of Address Decoder T3 during addresses 0000 through 0FFF. ROM1 is the chip-select signal for Program Memory K/L1. When low, ROM1 allows K/L1 to be addressed and to pass data to buffer F2.

ROM2
The active-low Read-Only Memory Chip Select 2 signal is software-generated at pin 10 of Address Decoder T3 during addresses A000 through AFFF. ROM2 is the chip-select signal for Program Memory K/L2. When low, ROM2 allows K/L2 to be addressed and to pass data to buffer F2.

ROM3
The active-low Read-Only Memory Chip Select 3 signal is software-generated at pin 12 of Address Decoder T2 during addresses E000 through EFFF. ROM3 is the chip-select signal for Program Memory P1/1. When low, ROM3 allows P1/1 to be addressed and to pass data to buffer F2.

ROM6
The active-low Read-Only Memory Chip Select 6 signal is software-generated at pin 11 of Address Decoder T2 during addresses D000 through DFFF. ROM6 is the chip-select signal for Program Memory R/S1. When low, ROM6 allows R/S1 to be addressed and to pass data to buffer F2.

ROM8
The active-low Read-Only Memory Chip Select 8 signal is software-generated at pin 8 of gate P3 in the Address Decoder circuit during addresses E000 through EFFF. ROM8 is the chip-select signal for Program Memory T1. When low, ROM8 allows T1 to be addressed and to pass data to buffer F2.

T/WB
The Buffered Read/High/Write/Data Enable signal is generated at pin 10 of inverter F4 in the Microprocessor circuit. T/WB is gated with B2 and D1 by gates H4 and J4 to produce W/TWB in the Bit Map Data Buffers circuit. T/WB is gated with RAM, BTMD, and BTIDM by gate F3 to produce the enable signals for buffer T9 and multiplexers S9 and N9.

W/RE
The Buffered Read/High/Write/Data Enable signal is generated by Microprocessor C2, buffered by E3, and applied to custom audio chips B1C3 and C10D of the Audio Output circuit and buffer E2 of the Microprocessor circuit. W/RE determines the direction of data flow through these devices.

SGC0/SGC4
The Planet Code Bit codes on lines SGC0-SGC4 are hardware-generated by counter M7 in the Planet ROM Address Generator circuit. The bit on line SGC0 is hardware-generated at pin 5 of latch E5. The Planet Segment Code provides the address bits for the Planet Picture ROM.

STARTLG
The active high-level Starting Longitude Enable signal is software-generated at pin 5 of latch E5. The Planet Segment Code provides the address for the Planet Picture ROM.

VSSEG
The active low-level Valid Segment signal is generated at pin 9 of latch E5. The active-low Valid Segment signal is generated at pin 9 of latch E5. The Planet Segment Code provides the address for the Planet Picture ROM.

W/DIS
Watching Disable is a test point at pin 1 of gate L4 in the Watchdog Circuit. When W/DIS is grounded, RESET is prevented from going to an active low level (except when the RESET test point is grounded).

VBLANK
The active high-level Vertical Blankening signal is hardware-generated at pin 11 of latch M4 in the Vertical Sync Circ. VBLANK is applied to multiplexers M11 in the Coin Door and Control Panel Input circuit. When RD0 is low and A80 is high, VBLANK is used by Microprocessor C2 on data bus line D8.

VBLS
The active low-level Vertical Blankening signal is hardware-generated at pin 10 of latch M4 in the Vertical Sync Circuit. VBLSN is used by Multiplexers M11 in the Coin Door and Control Panel Input circuit to produce VBLSN.

VC1KL, VC1L2
The Trak-Ball™ Vertical Clock signals are PCB input signals to the Trak-Ball™ Input circuit. When TBWSPW is high, VC1L2 is the clock signal for latch L11 and counter N11 in the Coin Door and Control Panel Input circuit. When TBWSPW is low, VC1KL is the clock signal for latch L11 and counter N11.

VDR1, VDR2
The Trak-Ball™ Vertical Direction signals are PCB input signals to the Trak-Ball™ Input circuit. When TBWSWP is high, VDR1 enables counter N11 in the Coin Door and Control Panel Input circuit to count; when TBWSWP is low, VDR2 enables counter N11.

VIRBLANK
The active low-level Video Blankening signal is hardware-generated at pin 6 of latch L4 in the Horizontal Sync Circuit. VIRBLANK is the clear signal for Color Memory latches A11 and D11.

VPLA
The active low-level Vertical Planet Enable signal is hardware-generated at pin 2 of latch M4 in the Vertical Sync Circuit. VPLA is gated with PISSG by gate R4 in the Planet Control circuit to produce the clear signal for latch D9.

VSYNC
The active high-level Vertical Synchronization signal is hardware-generated at pin 8 of latch M4 in the Vertical Sync Circuit. VSINC is exclusive-ORed with VSINC by gate M3 to produce COUNTER. VSINC is used directly to the video display circuitry for further processing.

W/DIS
Watching Disable is a test point at pin 1 of gate L4 in the Watchdog Circuit. When W/DIS is grounded, RESET is prevented from going to an active low level (except when the RESET test point is grounded).

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Liberator™ PCB Signal Name Descriptions

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1st Printing
Description of Liberator PCB Signal Names (continued)

WDD3
The active low-level Watchdog signal is software-generated at pin 6 of Address Decoder S2. WDD3 is gated with WDD1 by gate L4 in the Watchdog circuit to produce the load signal for counter J11 of the Power-On Reset circuit.

WTP-03
The active low-level Write Pulses 0-3 are software-generated from gate B5 in the Write Protection circuit. These pulses are the write enable signals for the Bit Map Memories.

WRITE
The active low-level Write Enable signal is hardware-generated at pin 11 of gate J4 in the Microprocessor circuit. WRITE is applied to gate H3 in the Bit Map Address Decoders circuit where it is used to develop YCOORD and XCOORD. In the Write Protection circuit, WRITE is gated with RAM by gate N4 to produce the clear signal for latch D5. In the Address Decoders circuit, WRITE is applied to gate H3 to produce the D input signal for decoder S2.

X-07X
The Planet Scaling bits are generated by latches F6 and D10 in the Multiplier circuit. Each of these bits is developed by those from the Longitude and Latitude Scaling circuits in the Inland Segment Detector, the bits on K0 and those from LCO1 and LCO2 are summed to produce WAVED from the carry bit of adder F7.

XCOORD
The active high-level Pixel X Coordinate signal is software-generated at pin 3 of timer A in the Bit Map X Decoders circuit during address 0000. XCOORD is the clock signal for Bit Map Decoder F1. When XCOORD goes high, it internally latches the data bits from D80-D87. Then, when BITMAP goes low, these bits are output from F1 to lines PIX0-PIX7 and ADD-ADD15.

YCOORD
The active high-level Pixel Y Coordinate signal is software-generated at pin 11 of gate H3 in the Bit Map Address Decoders circuit during address 0000. YCOORD is the clock signal for Bit Map Decoder H1. When YCOORD goes high, it internally latches the data bits from D80-D87. Then, when BITMAP goes low, these bits are output from H1 to lines ADD16-ADD19.

Horizontal Timing Signal 1 is hardware-generated at pin 10 of latch D9 in the Horizontal Sync Chain. H1 is ANDed with SMP2 by gate F8 of the Refresh circuit for use in developing RAM. In the Multiplock Circuit, H1 is ANDed with H3 by gate F8 to produce the clear signal for latch D8. H1 is the clock signal for latch K3 of the Valence Segment Detector, and its associated circuitry, that is exclusive-ORed with the output signal at pin 14 of latch S4 by gate M3.

Horizontal Timing Signal 1 is hardware-generated at pin 9 of latch D9 in the Horizontal Sync Chain. In the Microprocessor circuit, H1 is gated with B40 and B42 by gates H4 and J4 to produce WRITE. H1 is NANDed with J46 by gate N4 of the Load Raster Control Circuit to develop the input signal for latch K3.

5MHz
The 5 MHz clock signal is hardware-generated at pin 5 of Clock latch C3. SM52 is the P enable signal for counters E9 and F9 in the Horizontal Sync Chain. In the Refresh circuit, SM52 is ANDed with H1 by gate F8. SM52 is the clock signal for Load Raster Control Latch K3 and Planar Control latch H5.

5MHz
The Complementary 5 MHz clock signal is hardware-generated at pin 8 of Clock latch C8. SM52 is the input signal for latch D8 in the Write Protection circuit. 5MHz is the clock signal for Bit Map Shift Registers M9, P9, and P10. In the Multiplock Circuits, 5MHz is the input signal for latches D8 and C8. In the Planar Circuit 5MHz is the clock signal for latch D8. SM52 is gated with VREAD and LDRAST by gates N4 and P4 in the Line Buffer Address Control in the Base RAM circuit. 5MHz is gated with BITMAP in J3 to produce the write enable signal for Base RAM L5. In the Color Memory, 5MHz is the clock signal for latches H5 and D5. It is also gated with COLORRAM by gate P9 to produce the write enable signal for Color RAMS B11, C71, E11, and F11.

10MHz
The 10 MHz clock signal is hardware-generated at pin 9 of Clock latch BB. The 10 MHz signal is used to clock latches E9 and F9 in the Refresh circuit, D8 of the Multiplock Circuits, and D5 of the Write Protection circuit. 10MHz is ANDed with B9 by gate F9 in the Horizontal Sync Chain to produce the clock signal for latch T4. In the Multiplock Circuit 10MHz is used by latch C3 to produce the CURLOWE and PLUS signals. In the Display Signal and Comparator circuit, 10MHz is gated with L52ANC by gate B9 to produce the latch TS.

10MHz
The Complementary 10 MHz clock signal is hardware-generated at pin 8 of Clock latch BB. 10MHz is the clock signal for latch C9 in the Refresh circuit, devices D9, E9, and F9 in the Horizontal Sync Chain; counters B6 and D6 in the Display Counter and Comparator; and counters D11 and D11 in the Color Memory. In addition, 10MHz is gated with 20MHz by gate B9 of the Display Counter and Comparator to produce the clock signal for Hip-K4.

20MHz
The 20 MHz clock signal is hardware-generated by crystal clock Y1 in the Clock Circuit. 20MHz is the clock signal for latches B8 in the Clock Circuit and the Display Counter and Comparator. 20MHz is gated with 10MHz by gate B9 to produce the clock signal for Hip-K4.

20MHz
The Complementary 20 MHz clock signal is hardware-generated at pin 4 of inverter A8 in the Clock Circuit. 20MHz is the clock signal for latches O8 and D8 of the Multiplock Circuit.

Vertical Timing Signal 1 is hardware-generated at pin 14 of counter J8 in the Vertical Sync Chain. 1V and 2V are multiplexed by gate K8 and latched by M4 to produce VBLANK and VBLANK. Also, 1V is used by latch L8 to produce YDLV. 1V is multiplexed with 12V, AB13, and AB14 by Bit Map Address Multiplexer L9.

Vertical Timing Signal 2 is hardware-generated at pin 13 of counter J8 in the Vertical Sync Chain. 2V and 3V are multiplexed by gate K8 and latched by M4 to produce VSBYNC and VBLANK. Also, 2V is used by latch L8 to produce YDLV. 2V is multiplexed with 4H, AB7, and AB8 by Bit Map Address Multiplexer H9.

Vertical Timing Signal 4 is hardware-generated at pin 12 of counter J8 in the Vertical Sync Chain. 4V and 5V are multiplexed by gate K8 and latched by M4 to produce VSYN and VBLANK. Also, 4V is used by latch L8 to produce YDLV. 4V is multiplexed with 6H, AB8, and AB1 by Bit Map Address Multiplexer H9.

Vertical Timing Signal 6 is hardware-generated at pin 11 of counter J8 in the Vertical Sync Chain. 6V and 7V are multiplexed by gate K8 and latched by M4 to produce VSYN and VBLANK. Also, 6V is used by latch L8 to produce YDLV. 6V is multiplexed with 16H, AB8, and AB12 by Bit Map Address Multiplexer J9.

Vertical Timing Signal 16 is hardware-generated at pin 14 of counter J8 in the Vertical Sync Chain. 16V and 32V are multiplexed by gate K8 and latched by M4 to produce YIRL and VIRL. Also, 16V is used by latch L8 to produce YDLV. 16V is multiplexed with 32H, AB13, and AB14 by Bit Map Address Multiplexer J9.

Vertical Timing Signal 32 is hardware-generated at pin 13 of counter J8 in the Vertical Sync Chain. 32V and 64V are multiplexed by gate K8 and latched by M4 to produce YIRL and VIRL. Also, 32V is used by latch L8 to produce YDLV. 32V is multiplexed with 64H, AB12, and AB14 by Bit Map Address Multiplexer K9.

Vertical Timing Signal 64 is hardware-generated at pin 12 of counter J8 in the Vertical Sync Chain. 64V and 128V are multiplexed by gate K8 and latched by M4 to produce YIRL and VIRL. 64V is multiplexed with 128H, AB13, and AB14 by Bit Map Address Multiplexer K9.

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Description of Liberator PCB Signal Names (continued)

64V
Complementary Vertical Timing Signal 64V is hardware-generated at pin 8 of inverter A8 in the Vertical Sync Chain. 64V is used by latch LB in the Vertical Sync Chain.

128V
Vertical Timing Signal 128V is hardware-generated at pin 11 of counter A11 in the Vertical Sync Chain. 128V and 64V are multiplexed by K6 and latched by M4 to produce VPLA. 128V is the clock 1 signal for counter J1 of the Power-On Reset circuit. 128V is also multiplexed with Y, AB13, and A86 by Bit Map Address Multiplexor U4. 128V is applied with AB3 to Base RAM decoder U7 to generate address bit 4 for Base RAM L5.

1VDL
Delayed Vertical Timing Signal 1 is hardware-generated at pin 5 of latch LB in the Vertical Sync Chain. 1VDL is derived from 1V after a delay by HBLANK. 1VDL is address bit 5 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 0 for Latitude Scalers P8 and N8.

2VDL
Delayed Vertical Timing Signal 2 is hardware-generated at pin 15 of latch LB in the Vertical Sync Chain. 2VDL is derived from 2V after a delay by HBLANK. 2VDL is address bit 6 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 1 for Latitude Scalers P8 and N8.

4VDL
Delayed Vertical Timing Signal 4 is hardware-generated at pin 9 of latch LB in the Vertical Sync Chain. 4VDL is derived from 4V after a delay by HBLANK. 4VDL is address bit 7 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 2 for Latitude Scalers P8 and N8.

8VDL
Delayed Vertical Timing Signal 8 is hardware-generated at pin 6 of latch LB in the Vertical Sync Chain. 8VDL is derived from 8V after a delay by HBLANK. 8VDL is address bit 8 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 3 for Latitude Scalers P8 and N8.

16VDL
Delayed Vertical Timing Signal 16 is hardware-generated at pin 2 of latch LB in the Vertical Sync Chain. 16VDL is derived from 16V after a delay by HBLANK. 16VDL is address bit 9 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 4 for Latitude Scalers P8 and N8.

32VDL
Delayed Vertical Timing Signal 32 is hardware-generated at pin 18 of latch LB in the Vertical Sync Chain. 32VDL is derived from 32V after a delay by HBLANK. 32VDL is address bit 10 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 5 for Latitude Scalers P8 and N8.

64VDL
Delayed Vertical Timing Signal 64V is hardware-generated at pin 12 of latch LB in the Vertical Sync Chain. 64VDL is derived from 64V after a delay by HBLANK. 64VDL is address bit 11 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 6 for Latitude Scalers P8 and N8.

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Liberator PCB Signal Name Descriptions

ATARI INC., 1982
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SP-209 Sheet 11-B
1983 Printing
Liberator™ Troubleshooting with the CAT Box

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Troubleshooting with the Read/Write Controller

A. CAT Box Preliminary Set-Up
1. Remove the electrical power from the game and the CAT Box.
2. Remove the wiring harness from the game PCB.
3. Remove the game PCB from the game cabinet.
4. Remove Microprocessor C2 from the game PCB.
5. Connect the harness from the game to the CAT Box.
6. Connect together the 40 and 42 test points on the game PCB with the shortest possible jumper.
7. Connect the WIRE test point to ground.
8. Connect the CAT Box flex cable to the game PCB edge test connector.
9. Apply power to the game and to the CAT Box.
10. Set CAT Box switches as indicated:
    a. TESTER SELF-TEST: OFF
    b. TESTER MODE: R/W
11. Press TESTER RESET.
12. Connect the DATA PROBE to the CAT Box. Connect the DATA PROBE ground clip to a game PCB ground test point.

NOTE: To avoid faulty readings while performing these troubleshooting tests, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

B. Checking the Address Lines
1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. PULSE MODE: UNLATCHED
   c. R/W MODE: OFF
   d. R/W: READ
3. Key in the address pattern given in Table 1 (use AAAAA to start) with the CAT Box keyboard.
4. Set R/W MODE to STATIC.
5. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 1 lights up. Repeat this step for each address line listed in Table 1.
6. Repeat parts 2-c through 5 using address 5555 in part 3.

C. Checking the Data Lines
1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: ADDR
   b. BYTES: 1024
   c. R/W MODE: OFF
   d. R/W: WRITE
3. Key in address 0000 with the keyboard.
4. Press DATA SET. Key in data 1A4 with the keyboard.
5. Set R/W MODE to PULSE and back to (OFF).
6. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 2 lights up. Repeat this check for each IC-pin in Table 2.
7. Repeat parts 4 through 6 using data 55 in part 4.

D. Checking the RAM
1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: ADDR
   b. BYTES: 1024
   c. R/W MODE: OFF
   d. R/W: WRITE
3. Enter address 0002 with the keyboard.

NOTE: Addresses 0000, 0001, and 0002 are special RAM locations for bit mode operation that cannot be verified by this RAM test.

Continued on back of sheet

Table 1: Address Lines

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Liberator™ PCB Troubleshooting

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SP-209 Sheet 12A
1st Printing
4. Set the CAT Box switches as indicated:
   a. R/W MODE to PULSE and back to (OFF)
   b. R/W TO READ
   c. R/W MODE to PULSE and back to (OFF)

5. If the CAT Box reads an address that doesn't compare with that written, the COMPARE ERROR LED will light up. The ADDRESS/SIGNATURE display of the CAT Box will show the failing address location and the ERROR DATA DISPLAY switch is enabled. Using this switch, determine if the error is in the high-order or low-order RAM.

6. Repeat parts 2 through 4 using addresses 0400, 0800, 0C00, 1000, 1400, 1800, 1200, 2000, 2400, 2800, 2C00, 3000, 3400, 3800, and 3C00.

7. Repeat this test with DBUS SOURCE set to ADDR.

E. Checking the Custom Audio I/O Chips

NOTE
Liberator has two custom audio I/O chips. Each must be tested separately. Here are several ways to test these chips:

- Perform the self-test.
- Substitute a known good part for a suspected defective part.
- Use the following procedure.

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/W WRITE
   c. R/W MODE: (OFF)
3. Enter the address from Table 3 with the keyboard.
4. Press DATA SET and enter the data from Table 3 with the keyboard.
5. Set R/W MODE to PULSE and back to (OFF).
6. Repeat parts 3 through 5 for each address and data listed in Table 3. Check for the response indicated.

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
<th>TEST RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>7800</td>
<td>00</td>
<td></td>
</tr>
<tr>
<td>780F</td>
<td>03</td>
<td></td>
</tr>
<tr>
<td>7800</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td>7801</td>
<td>AF</td>
<td>Custom Audio I/O Chip B3 channel 1 produces pure tone.</td>
</tr>
<tr>
<td>7802</td>
<td>00</td>
<td>Custom Audio I/O Chip B3 channel 1 off.</td>
</tr>
<tr>
<td>7803</td>
<td>55</td>
<td>Custom Audio I/O Chip B3 channel 2 produces pure tone.</td>
</tr>
<tr>
<td>7801</td>
<td>AF</td>
<td>Custom Audio I/O Chip B3 channel 2 off.</td>
</tr>
<tr>
<td>7800</td>
<td>00</td>
<td>Custom Audio I/O Chip B3 channel 3 produces pure tone.</td>
</tr>
<tr>
<td>780F</td>
<td>00</td>
<td>Custom Audio I/O Chip B3 channel 3 off.</td>
</tr>
<tr>
<td>7800</td>
<td>55</td>
<td>Custom Audio I/O Chip B3 channel 4 produces pure tone.</td>
</tr>
<tr>
<td>7801</td>
<td>AF</td>
<td>Custom Audio I/O Chip B3 channel 4 off.</td>
</tr>
<tr>
<td>7800</td>
<td>00</td>
<td>Custom Audio I/O Chip C/D3 channel 1 produces pure tone.</td>
</tr>
<tr>
<td>780F</td>
<td>00</td>
<td>Custom Audio I/O Chip C/D3 channel 1 off.</td>
</tr>
<tr>
<td>7802</td>
<td>55</td>
<td>Custom Audio I/O Chip C/D3 channel 2 produces pure tone.</td>
</tr>
<tr>
<td>7803</td>
<td>00</td>
<td>Custom Audio I/O Chip C/D3 channel 2 off.</td>
</tr>
</tbody>
</table>

F. Checking the Player Switch, Option Switch, and Trak-Ball™ Inputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/W WRITE
   c. R/W MODE: (OFF)
3. Enter address 6C04 with the keyboard.
4. Press DATA SET and enter data 00 with the keyboard.
5. Set R/W MODE to PULSE and back to (OFF). The CTRLD signal is now set to the low state.
6. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/W READ

7. For each address listed in Table 4, do the following:
   a. Set R/W MODE to (OFF).
   b. Enter the address with the keyboard.
   c. Set R/W MODE to STATIC.
   d. Activate the input switch indicated in Table 4 for the address and check the test result.

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>INPUT SWITCH</th>
<th>TEST RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>5000</td>
<td>Slam, Right coin switch, Left coin switch, SelfTest switch, Auxiliary coin switch</td>
<td>DATA display changes when any coin or self-test switch is activated.</td>
</tr>
<tr>
<td>5001</td>
<td>FIRE 1, SHIELD 1, FIRE 2, SHIELD 2, START 1, START 2</td>
<td>DATA display changes when any of these switches is activated. (Note display changes also without activating a switch because of YBLANK).</td>
</tr>
</tbody>
</table>

G. Checking the LED and Coin Counter Outputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. BYTES: 1
   c. R/W WRITE
   d. R/W MODE: (OFF)

CAUTION
If you write ON data to activate a solenoid, do not activate the solenoid immediately by writing the OFF data. If you leave a solenoid activated for more than 10 seconds, you may lose the solenoid and/or its driver, due to overheating.

3. For each address listed in Table 6, do the following:
   a. To activate the output:
      - Press DATA SET.
      - Enter data 00 with the keyboard.
      - Set R/W MODE to STATIC and back to (OFF).
   b. To deactivate the output:
      - Press DATA SET.
      - Enter data FF with the keyboard.
      - Set R/W MODE to STATIC and back to (OFF).

Continued on next sheet
Table 6 LED and Coin Counter Outputs

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA 0</th>
<th>DATA 1</th>
<th>OUTPUT DEVICE</th>
</tr>
</thead>
<tbody>
<tr>
<td>6C00</td>
<td>ON</td>
<td>OFF</td>
<td>Player 1 LED</td>
</tr>
<tr>
<td>6C01</td>
<td>ON</td>
<td>OFF</td>
<td>Player 2 LED</td>
</tr>
<tr>
<td>6C04</td>
<td>LOW</td>
<td>HIGH</td>
<td>CTRD</td>
</tr>
<tr>
<td>6C05</td>
<td>ON</td>
<td>OFF</td>
<td>Coin Counter Right</td>
</tr>
<tr>
<td>6C06</td>
<td>OFF</td>
<td>ON</td>
<td>Coin Counter Left</td>
</tr>
<tr>
<td>6C07</td>
<td>OFF</td>
<td>ON</td>
<td>PLANET</td>
</tr>
</tbody>
</table>

Troubleshooting with Signature Analysis

A. Checking the Address Lines and Address Decoders

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. BYTES: 1
   c. R/W: WRITE
   d. R/W MODE: OFF
3. Enter address 0000 with the keyboard.
4. Press DATA SET and enter data 08 with the keyboard.
5. Set R/W MODE to start and back to (OFF).
6. Enter address 0001 with the keyboard.
7. Press DATA SET and enter data 00 with the keyboard.
8. Set R/W MODE to STATIC and back to (OFF).
9. Connect the three BNC-to-EZ clip cables supplied with the CAT Box to the SIGNATURE ANALYSIS CONTROL, START, STOP, and CLOCK jacks of the CAT Box.
10. Connect the three black EZ clips to a game PCB ground test point.
11. Ground pin 4 of IC H4 (the DISDAT signal) on the game PCB.
12. Set the CAT Box switches as indicated:
    a. TESTER MODE: SIG
    b. TESTER SELF-TEST: OFF
    c. PULSE MODE: LATCHED
    d. START: Negative-going edge trigger
    e. STOP: Negative-going edge trigger
    f. CLOCK: Negative-going edge trigger
13. Press TESTER RESET on the CAT Box.
14. Connect the CAT Box Signature Analysis probe tips as indicated:
    a. START: Pin 3 of IC T2
    b. STOP: Pin 3 of IC T2
    c. CLOCK: 42 test point
15. Verify the set-up connections by connecting the DATA PROBE to a game PCB ground test point. The CAT Box ADDRESS/SIGNATURE display should show 0000. Now connect the DATA PROBE to a 4.5V test point. The ADDRESS/SIGNATURE display should show 0001.
16. Probe the IC pin listed in Table 7 with the DATA PROBE and check for the signature indicated. Repeat this check for each IC pin listed.

Table 7 Address Bus Signatures

<table>
<thead>
<tr>
<th>IC-PIN</th>
<th>SIGNAL NAME</th>
<th>SIGNATURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>E1-18</td>
<td>A82</td>
<td>U806U</td>
</tr>
<tr>
<td>E1-16</td>
<td>A81</td>
<td>5550</td>
</tr>
<tr>
<td>E1-14</td>
<td>A80</td>
<td>CCCC</td>
</tr>
<tr>
<td>E1-12</td>
<td>A83</td>
<td>777F</td>
</tr>
<tr>
<td>E1-11</td>
<td>A84</td>
<td>5H21</td>
</tr>
<tr>
<td>E1-10</td>
<td>A85</td>
<td>0AFA</td>
</tr>
<tr>
<td>E1-9</td>
<td>A86</td>
<td>8FFH</td>
</tr>
<tr>
<td>E1-8</td>
<td>A87</td>
<td>53F8</td>
</tr>
<tr>
<td>E1-7</td>
<td>A88</td>
<td>HC96</td>
</tr>
<tr>
<td>E1-6</td>
<td>A89</td>
<td>2H10</td>
</tr>
<tr>
<td>E1-5</td>
<td>A8A</td>
<td>H990</td>
</tr>
<tr>
<td>E1-4</td>
<td>A8B</td>
<td>1203</td>
</tr>
<tr>
<td>E1-3</td>
<td>A8C</td>
<td>HAP7</td>
</tr>
<tr>
<td>E1-2</td>
<td>A8D</td>
<td>3C96</td>
</tr>
<tr>
<td>E1-1</td>
<td>A8E</td>
<td>3027</td>
</tr>
<tr>
<td>E1</td>
<td>A8F</td>
<td>755U</td>
</tr>
</tbody>
</table>

B. Checking the Planet-Generating Circuity

1. Perform steps 1 through 7 of the CAT Box preliminary set-up.
2. Connect the CAT Box Signature Analysis probe tips where indicated:
    a. START: Pin 11 of IC E9
    b. STOP: Pin 11 of IC E9
    c. CLOCK: Pin 8 of IC E8
3. Connect the ground clips of the CAT Box Signature Analysis and DATA probes to a game PCB ground test point.
4. Set the CAT Box switches as indicated:
    a. TESTER MODE: SIG
    b. TESTER SELF-TEST: OFF
    c. PULSE MODE: UNLATCHED
    d. START: Positive-going edge trigger
    e. STOP: Positive-going edge trigger
    f. CLOCK: Positive-going edge trigger
5. Turn on the game and the CAT Box.
6. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for A76F.
7. Test the signatures designated by (XXXX) printed in color on the schematic diagrams of the game PCB. To test for a signature, use the CAT Box DATA PROBE to probe the appropriate location on the game PCB. Then check the ADDRESS/SIGNATURE display for the appropriate signature.

NOTE
To avoid faulty readings while performing these troubleshooting tests, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

17. Probe the IC pin listed in Table 8 with the DATA PROBE and check for the signature indicated. Repeat this check for each IC pin listed.

Table 8 Decoder Signatures

<table>
<thead>
<tr>
<th>IC-PIN</th>
<th>SIGNAL NAME</th>
<th>SIGNATURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>E4-0</td>
<td>B1MD</td>
<td>4001</td>
</tr>
<tr>
<td>E4-8</td>
<td>B1TD</td>
<td>4000</td>
</tr>
<tr>
<td>E4-5</td>
<td>YCOORD</td>
<td>4001</td>
</tr>
<tr>
<td>E4-4</td>
<td>XCOORD</td>
<td>0000</td>
</tr>
<tr>
<td>E4-12</td>
<td>E0R</td>
<td>6F4H</td>
</tr>
<tr>
<td>E4-11</td>
<td>IN0</td>
<td>574H</td>
</tr>
<tr>
<td>E4-10</td>
<td>IN1</td>
<td>96F8</td>
</tr>
<tr>
<td>E4-9</td>
<td>IBS</td>
<td>5454</td>
</tr>
<tr>
<td>E4</td>
<td>RAX</td>
<td>5F0B</td>
</tr>
<tr>
<td>T3-13</td>
<td>ROM0</td>
<td>CAT1</td>
</tr>
<tr>
<td>T3-11</td>
<td>ROM1</td>
<td>HT59</td>
</tr>
<tr>
<td>T3-10</td>
<td>ROM2</td>
<td>A3UH</td>
</tr>
<tr>
<td>T3-09</td>
<td>ROM3</td>
<td>A1A6</td>
</tr>
<tr>
<td>H4-8</td>
<td>ROM</td>
<td>755U</td>
</tr>
<tr>
<td>T2-12</td>
<td>ROMX</td>
<td>A7H1</td>
</tr>
<tr>
<td>T2-11</td>
<td>ROMA</td>
<td>5AF5</td>
</tr>
<tr>
<td>P3-8</td>
<td>ROMX</td>
<td>P255</td>
</tr>
</tbody>
</table>

10. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for 1308.
11. Set the CAT Box CLOCK switch for a positive-going edge trigger and test the signatures designated on the schematics by (XXXX0).

NOTE
To avoid faulty readings while performing these troubleshooting tests, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

12. Connect the CAT Box Signature Analysis probe tips to:
    a. START: Pin 11 of IC J8
    b. STOP: Pin 11 of IC J8
13. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for A76F.
14. Test the signatures designated on the schematics by (XXXX).

NOTE
To avoid faulty readings while performing these troubleshooting tests, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

15. Set the CAT Box CLOCK switch for a negative-going edge trigger and test the signatures designated on the schematics by (XXXX0).
16. Remove the electrical power from the game and the CAT Box.
17. Connect the CAT Box Flex cable to the game PCB edge test connector and connect the game PCB PSBT test point to ground.
18. Apply power to the game and the CAT Box.

Continued on back of sheet

Liberator™ PCB Troubleshooting

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19. Set the CAT Box switches as indicated:
   a. TESTER MODE: R/W
   b. BYTES: 1
   c. R/W: WRITE
   d. R/W MODE: OFF
20. Press TESTER RESET.
21. Enter address 6800 with the keyboard.
22. Press DATA SET and enter data 00 with the keyboard.
23. Set R/W MODE to PULSE and back to (OFF).
24. Enter address 4007 with the keyboard and repeat steps 22 and 23.
25. Set the CAT Box switches as indicated:
   a. TESTER MODE: SIG
   b. START: Negative-going edge trigger
   c. STOP: Negative-going edge trigger
   d. CLOCK: Positive-going edge trigger
26. Connect the CAT Box Signature Analysis probe tips to:
   a. START: Pin 12 of IC L4
   b. STOP: Pin 12 of IC L4
   c. CLOCK: Pin 10 of IC A8
27. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for FF 96.
28. Test the signatures designated on the schematics by (XXX)94.

NOTE
To avoid faulty readings while performing these troubleshooting tests, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidentally occur, you must again perform the test from its start.

30. Set the CAT Box CLOCK switch for a negative-going edge trigger and test the signatures designated on the schematics by (XXX)94.
31. Press DATA SET and enter data 7F with the keyboard.
32. Press R/W MODE to PULSE and back to (OFF).
33. Set the CAT Box switches as indicated:
   a. TESTER MODE: SIG
   b. START: Positive-going edge trigger
   c. STOP: Negative-going edge trigger
   d. CLOCK: Positive-going edge trigger
34. Connect the CAT Box Signature Analysis probe tips to:
   a. START: Pin 2 of IC M4
   b. STOP: Pin 2 of IC M4

35. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for FF 96.
36. Test the signatures designated on the schematics by (XXX)95.

Troubleshooting with Checksums

NOTE
This procedure can only be done with those CAT Boxes equipped with a Checksum Switch.

CAUTION
While testing with checksums, adding 100 pF capacitors to A14 and A15 may be necessary.

1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as indicated:
   a. BYTES: 256
   b. DBUS SOURCE: DATA
   c. R/W MODE: OFF
   d. CHECKSUM SWITCH: ON
3. Key in the address pattern given in Table 9 (use address 8000 to start).
4. Set the R/W MODE switch to PULSE and then back to (OFF).
5. Check the CAT Box ADDRESS/SIGNATURE display for the appropriate checksum.
6. Repeat parts 3 through 5 for each address listed in Table 9.

Table 9 ROM Checksums

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>ROM TESTED</th>
<th>CHECKSUM</th>
</tr>
</thead>
<tbody>
<tr>
<td>8000</td>
<td>ROM0</td>
<td>2D29</td>
</tr>
<tr>
<td>9000</td>
<td>ROM1</td>
<td>EF0D</td>
</tr>
<tr>
<td>4000</td>
<td>ROM2</td>
<td>8065</td>
</tr>
<tr>
<td>6000</td>
<td>ROM3</td>
<td>17A9</td>
</tr>
<tr>
<td>C000</td>
<td>ROM4</td>
<td>E41F</td>
</tr>
<tr>
<td>0000</td>
<td>ROM5</td>
<td>55A7</td>
</tr>
<tr>
<td>E000</td>
<td>ROM6</td>
<td>B8E7</td>
</tr>
</tbody>
</table>

Troubleshooting the Watchdog Circuit

The Watchdog circuit will send continuous reset pulses to the microprocessor if a problem exists within the microprocessor circuit. If the self-test fails to run, it is a good practice to check the reset line.

RESET is a microprocessor input pin 40. In a properly operating system, reset should occur during power-up or when the RESET test point is grounded. A pulsing RESET line indicates something is causing the microprocessor to lose its place within the program. Typical causes are:

1. Open or shorted address or data bus lines.
2. Bad microprocessor chip.
3. Bad bus buffers.
4. Bad ROM.
5. Bad RAM.
6. Any bad input or output that causes an address or data line to be held in a constant high or low state.

A pulsing RESET signal indicates a problem somewhere within the microprocessor circuitry rather than within the analog vector-generator. To aid in troubleshooting, the MOSIS test point can be connected to a ground test point to prevent resets. This will sometimes allow the Self-Test to be used to diagnose the failure during a RESET condition.

Liberator™ PCB Troubleshooting

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WARNING

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Electrohome 19-Inch Color Raster-Scan Video Display Schematic Diagram

Schematic Notes
Unless otherwise specified:
- Resistance: [Ω] (kΩ = kΩ, M = MΩ), 1/4 (W) carbon resistor
- Capacitance: 1 or higher = (µF), less than 1 = (pF)
- Working voltage = 50 (V)
- Ceramic capacitor
- Inductance: (H)
- Electrolytic Cap: Capacity Value (µF)/(Working voltage (V))
- NP = Non-polar (or bipolar) electrolytic cap.

Refer to the parts list for additional component information.
- Indicates test point connection
- Indicates chassis ground unless otherwise specified
- Hz indicates cycles per second

For safety purposes (and continuing reliability)
- Replace all components marked with safety symbol with identical type.
- NOTE: FR = fused resistor

Parts identification on circuit boards:
e.g. SU1126A (R107 - R1107)
SU3030A (R113 - R1113)

WARNING
Components identified by shading have special characteristics important to safety and must be replaced only with identical parts.

Electrohome Color Raster Display Schematic

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